

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mohamed Azimane et al.

Group Art Unit: 2117

Application No.: 10/591,193

Examiner: McMahon, Daniel F.

Filed: August 30, 2006

Confirmation No.: 5900

For: DFT TECHNIQUE FOR STRESSING SELF-TIMED  
SEMICONDUCTOR MEMORIES TO DETECT DELAY  
FAULTS

Mail Stop RCE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SUBMISSION UNDER 37 C.F.R. 1.114

Sir:

In response to the Final Office Action mailed August 17, 2009, please find the following:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 8 of this paper.

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CERTIFICATE OF MAILING UNDER 37 C.F.R. 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

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